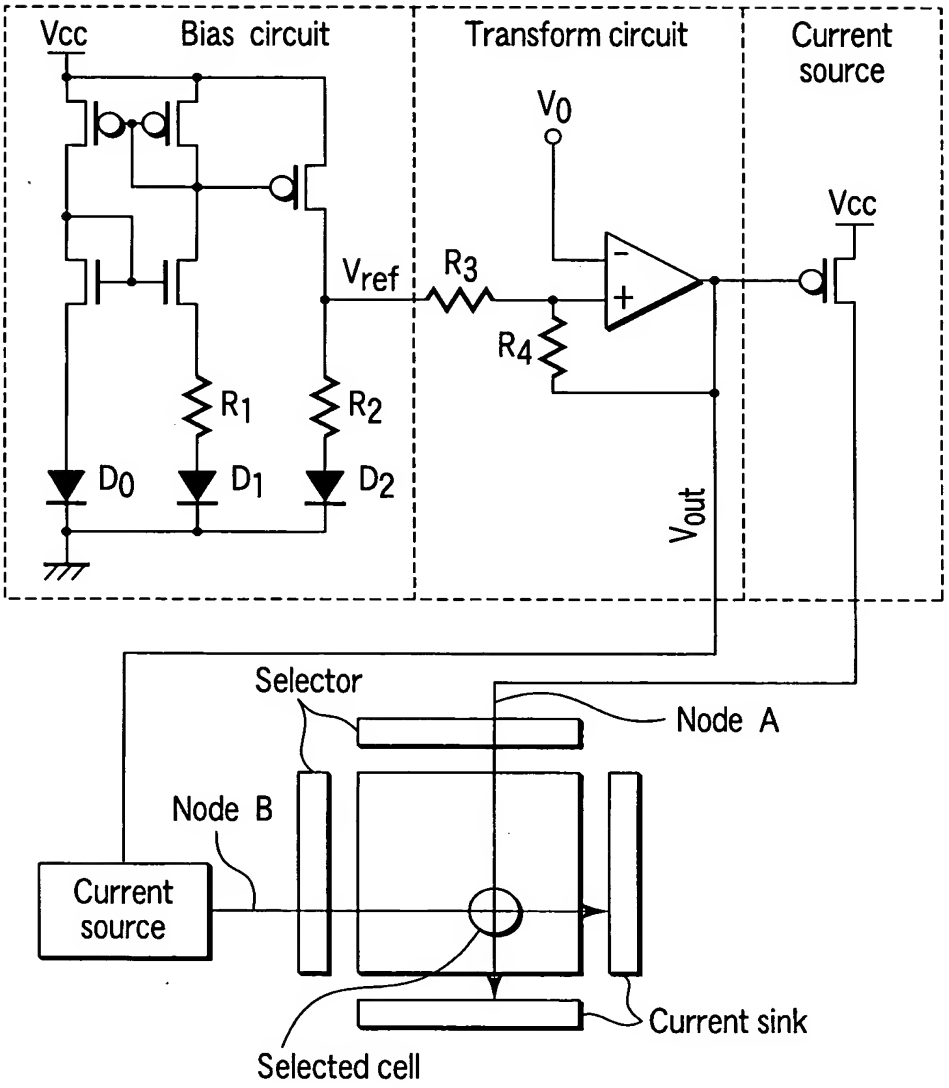

FIG. 1 PRIOR ART

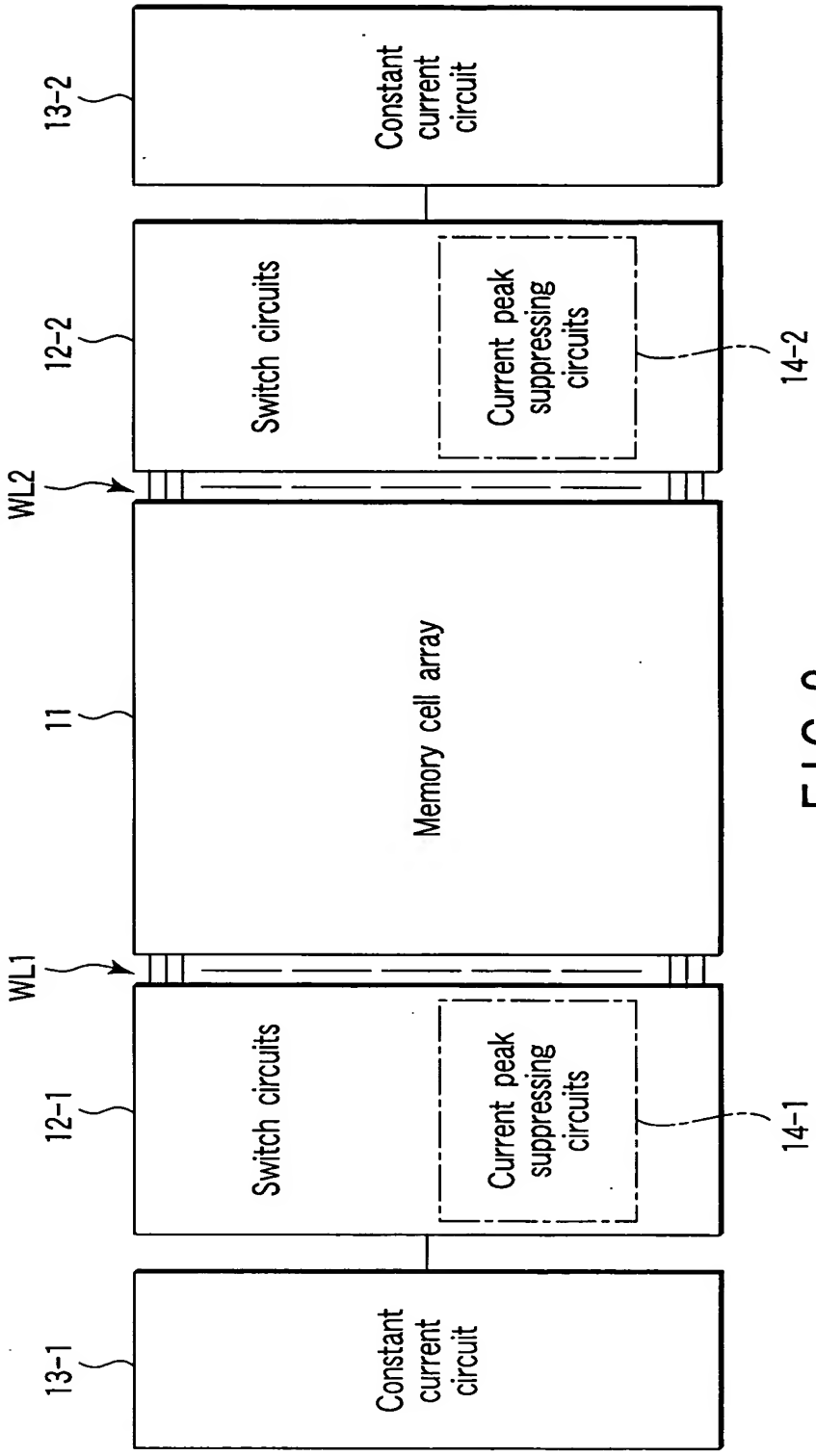
13-2
Constant current circuit
12-2
Switch circuits
Current peak suppressing circuits
14-2
WL2
11
Memory cell array
WL1
12-1
Switch circuits
Current peak suppressing circuits
14-1
13-1
Constant current circuit

FIG. 2

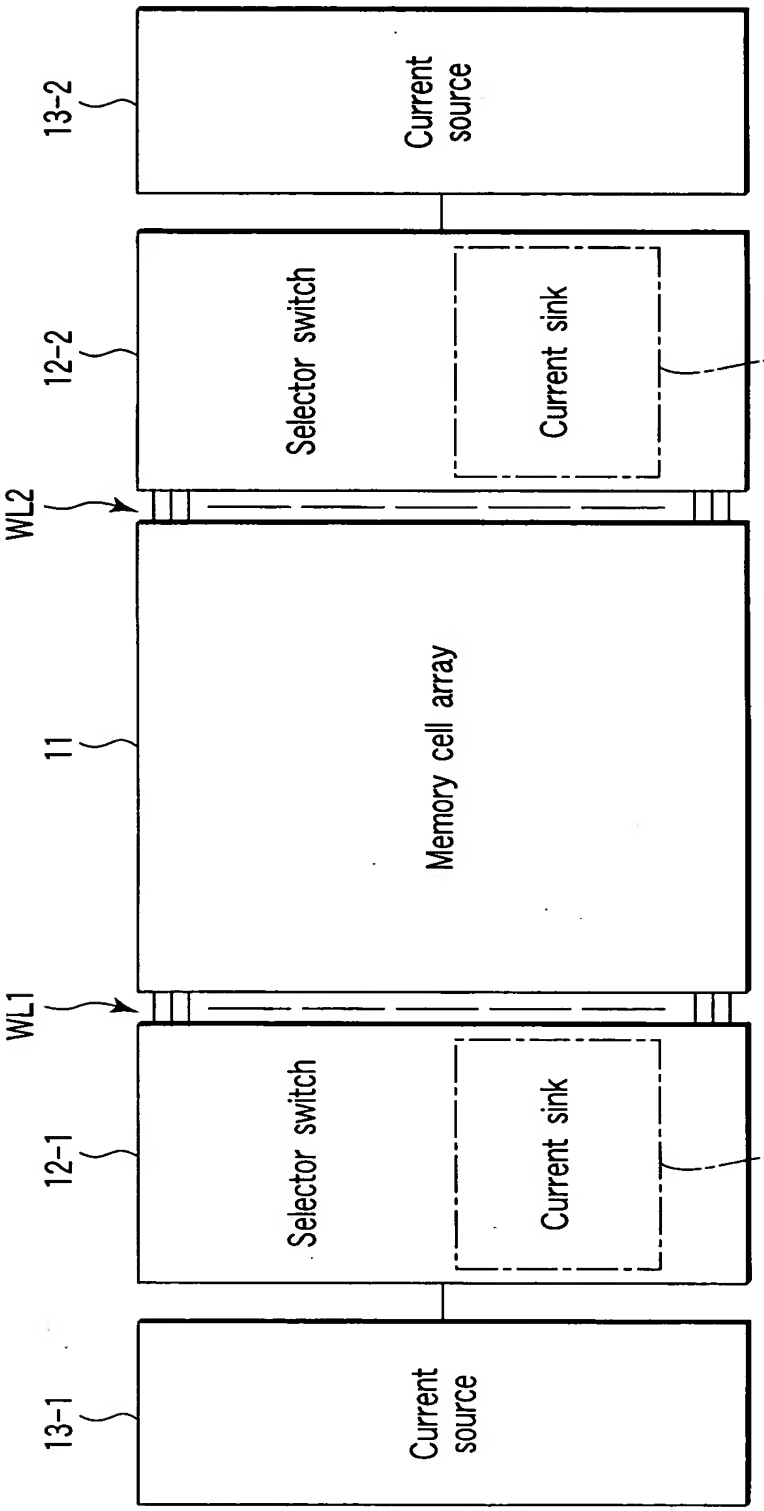
13-2
Current source
12-2
Selector switch
Current sink
14-2
WL2
11
Memory cell array
WL1
12-1
Selector switch
Current sink
14-1
13-1
Current source

FIG. 3

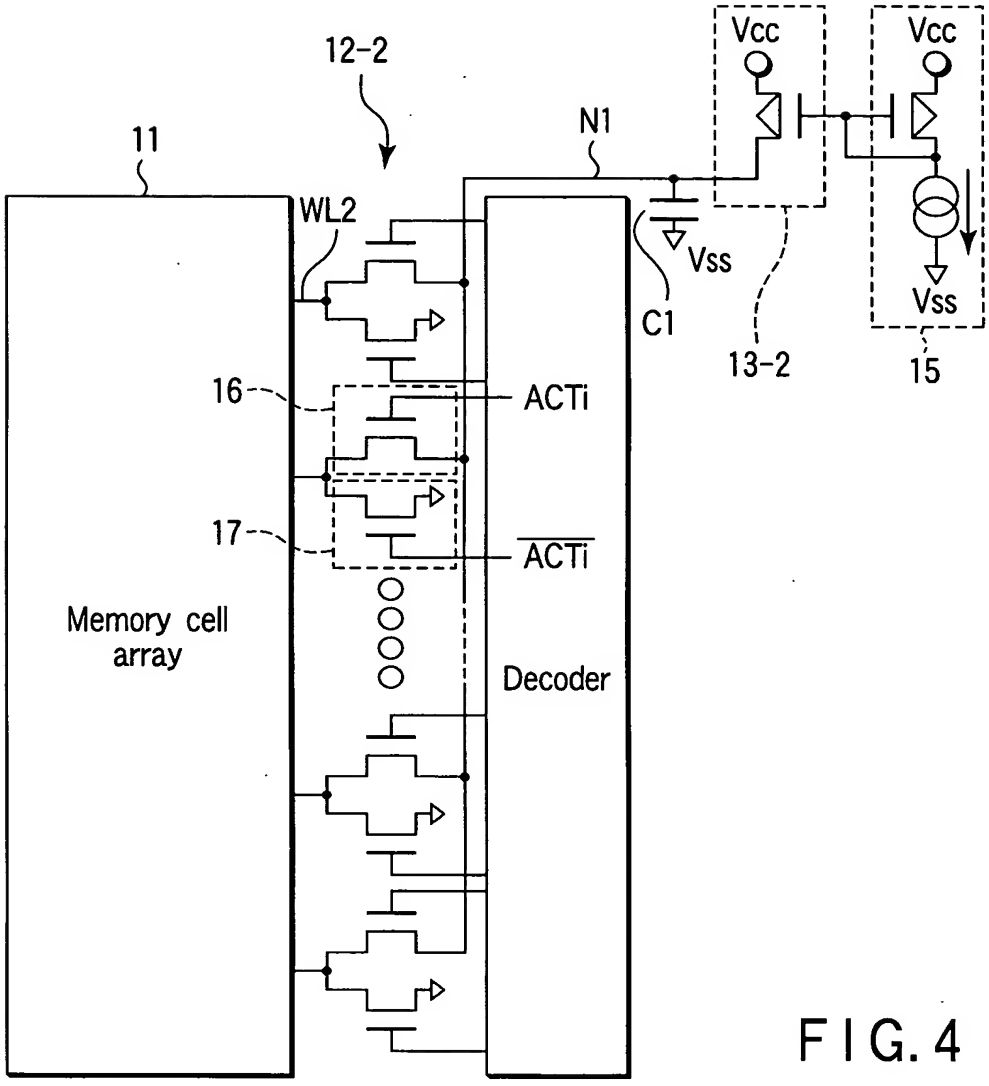

FIG. 4

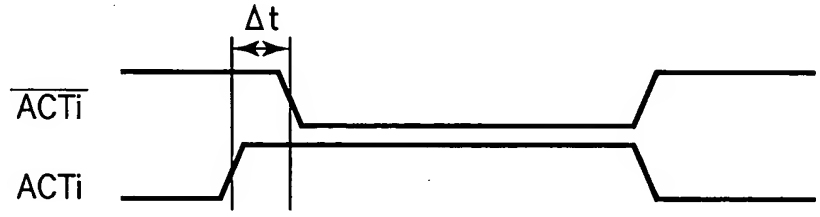

FIG. 5

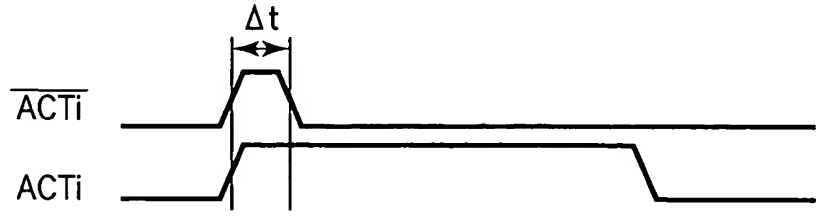

FIG. 6

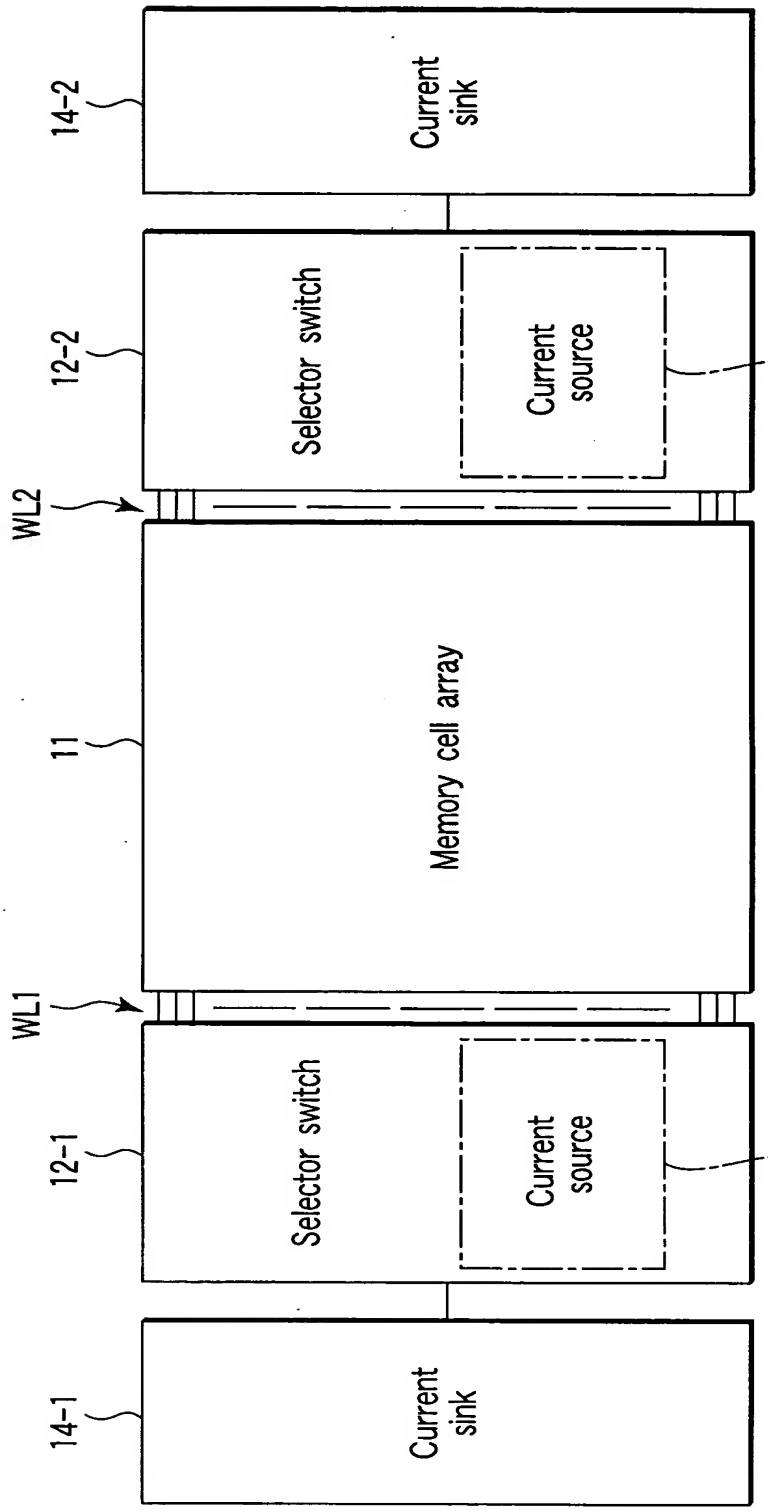
14-2
Current sink
12-2
Selector switch
Current source
13-2
WL2
11
Memory cell array
WL1
12-1
Selector switch
Current source
13-1
14-1
Current sink

FIG. 7

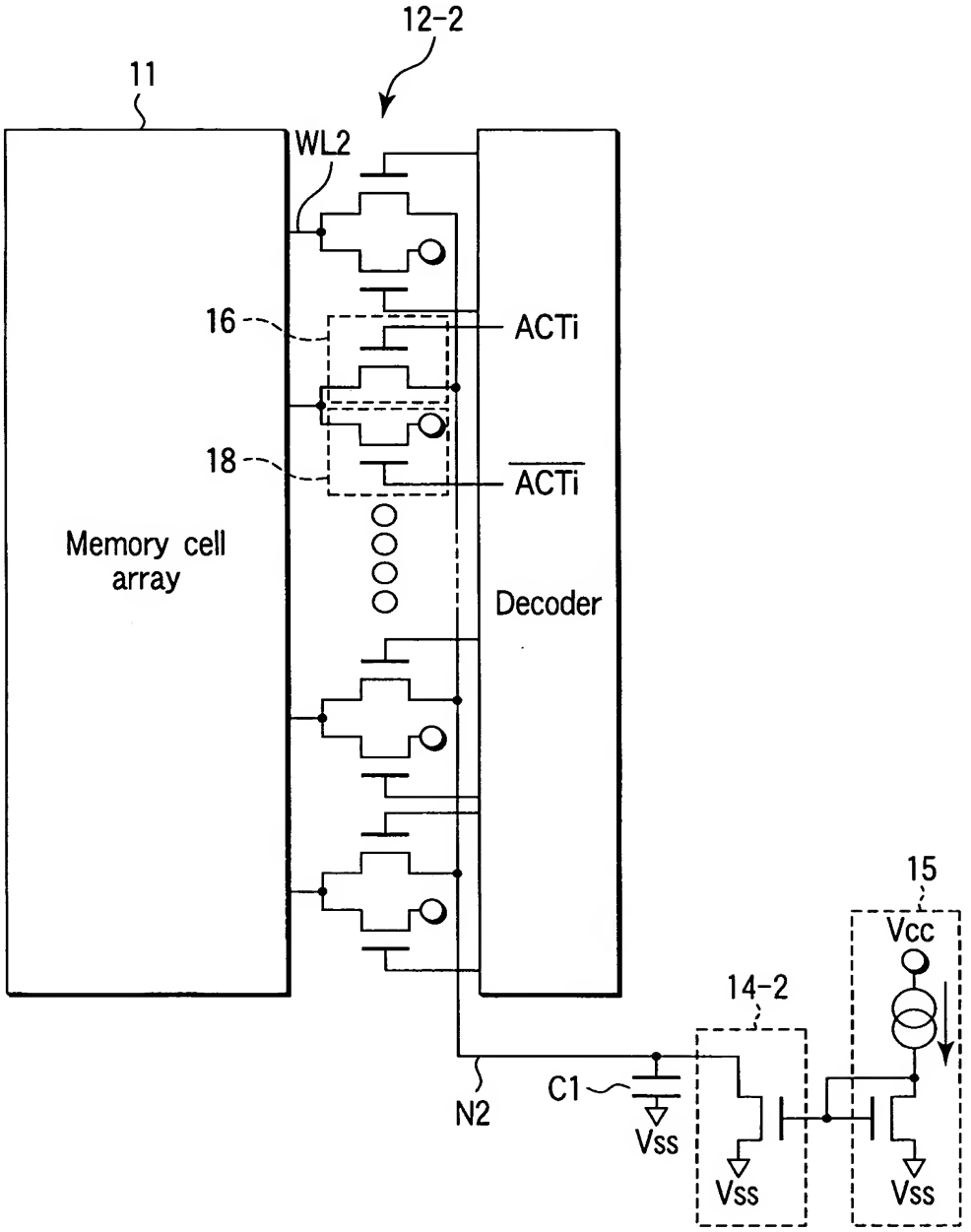
12-2
11
WL2
16
ACTi
18
$\overline{ACTi}$
Memory cell array
Decoder
15
Vcc
14-2
C1
N2
Vss
Vss
Vss

FIG. 8

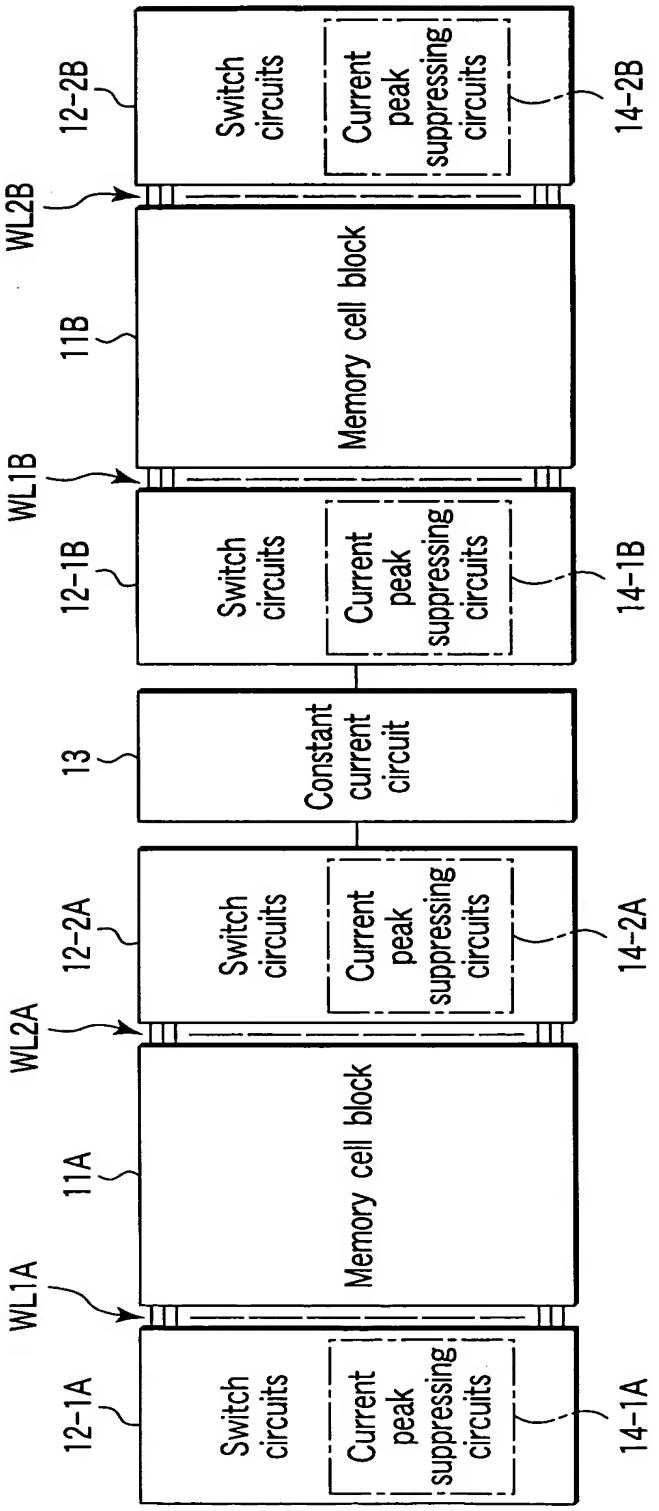
12-2B
Switch circuits
Current peak suppressing circuits
14-2B
WL2B
11B
Memory cell block
WL1B
12-1B
Switch circuits
Current peak suppressing circuits
14-1B
13
Constant current circuit
12-2A
Switch circuits
Current peak suppressing circuits
14-2A
WL2A
11A
Memory cell block
WL1A
12-1A
Switch circuits
Current peak suppressing circuits
14-1A

FIG. 9

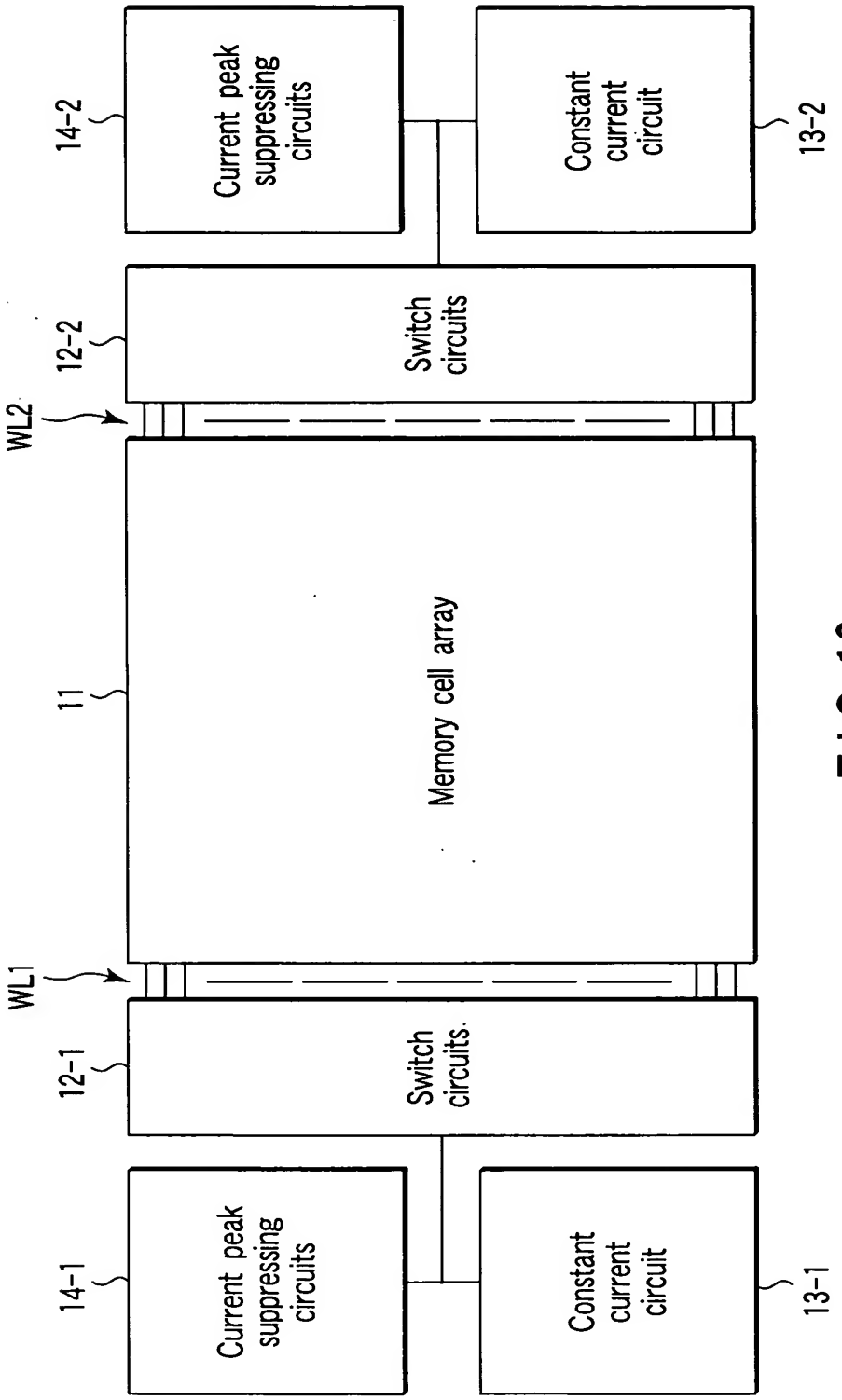
14-2
Current peak suppressing circuits
Constant current circuit
13-2
12-2
Switch circuits
WL2
11
Memory cell array
WL1
12-1
Switch circuits
14-1
Current peak suppressing circuits
Constant current circuit
13-1

FIG. 10

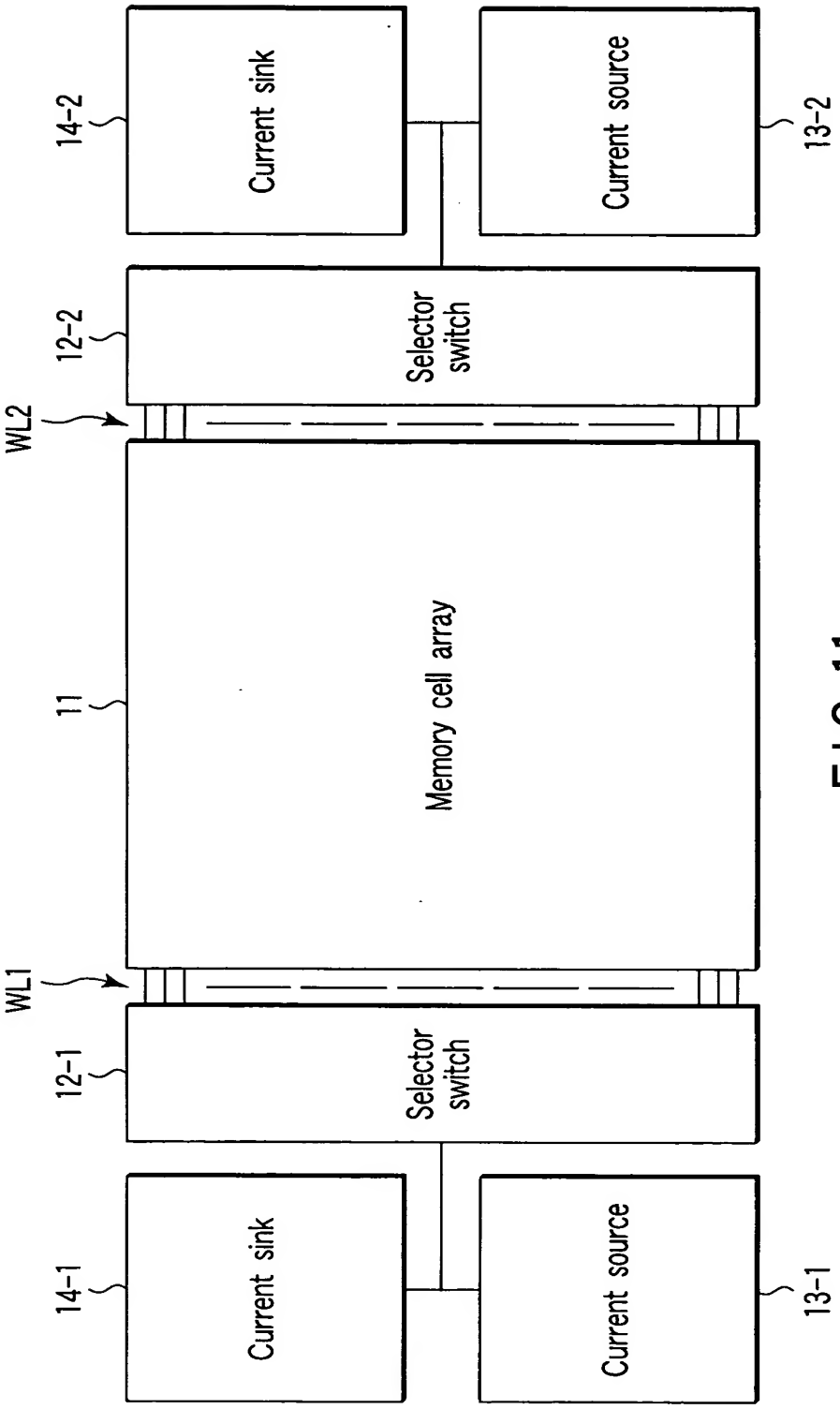
14-2
Current sink
Current source
13-2
12-2
Selector switch
WL2
11
Memory cell array
WL1
12-1
Selector switch
14-1
Current sink
Current source
13-1

FIG. 11

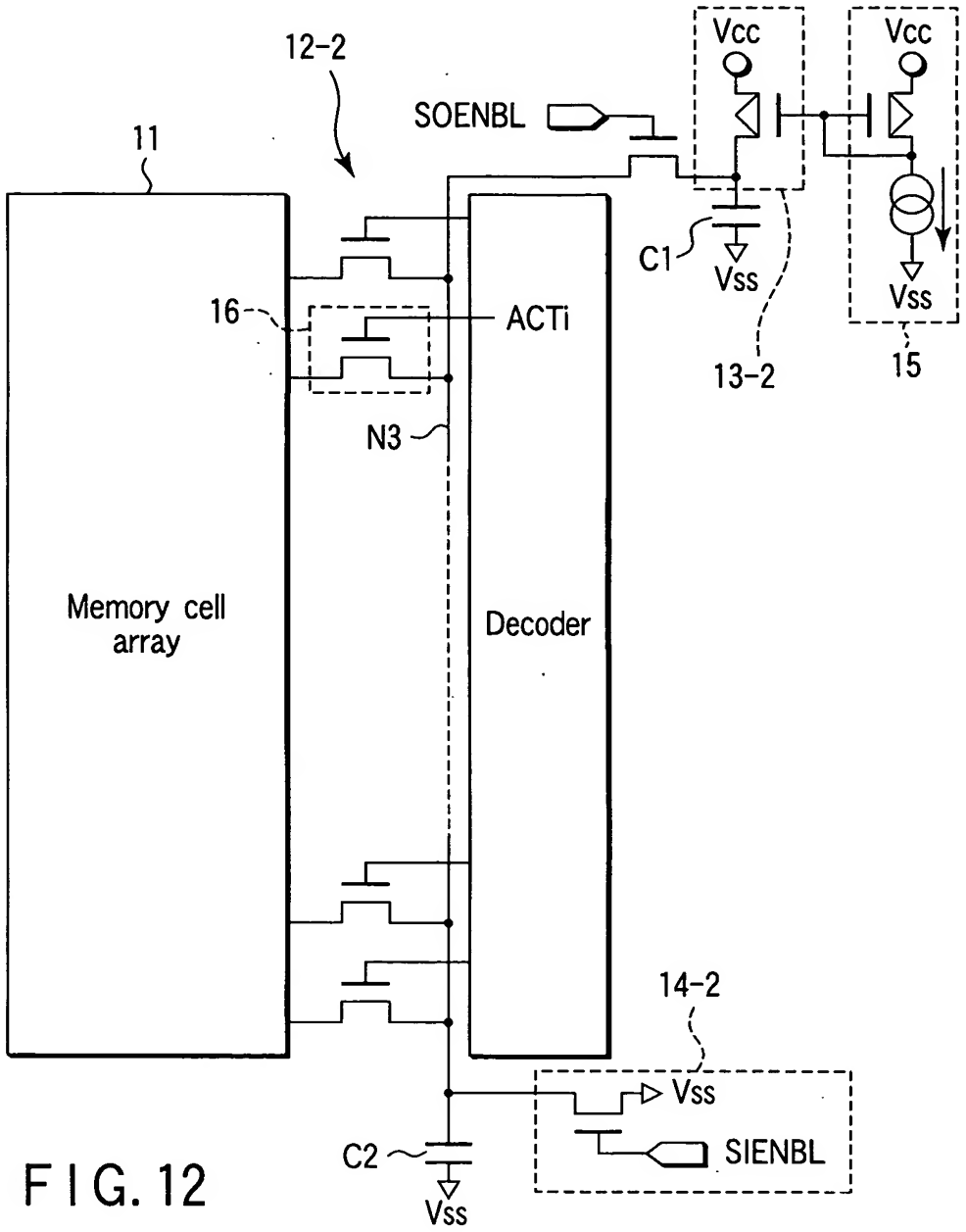
12-2
11
SOENBL
Vcc
Vcc
C1
Vss
Vss
16
ACTi
13-2
15
N3
Memory cell array
Decoder
14-2
Vss
SIENBL
C2
Vss

FIG. 12

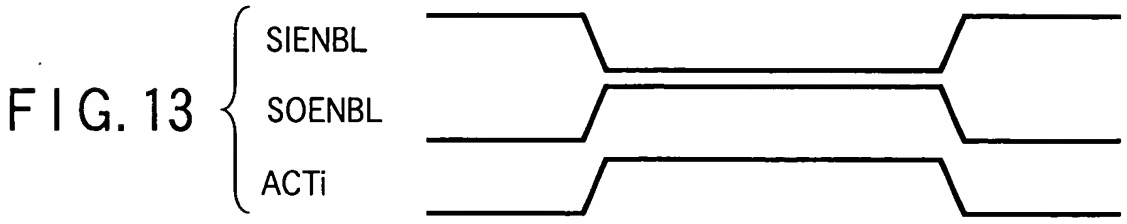
SIENBL
SOENBL
ACTi

FIG. 13

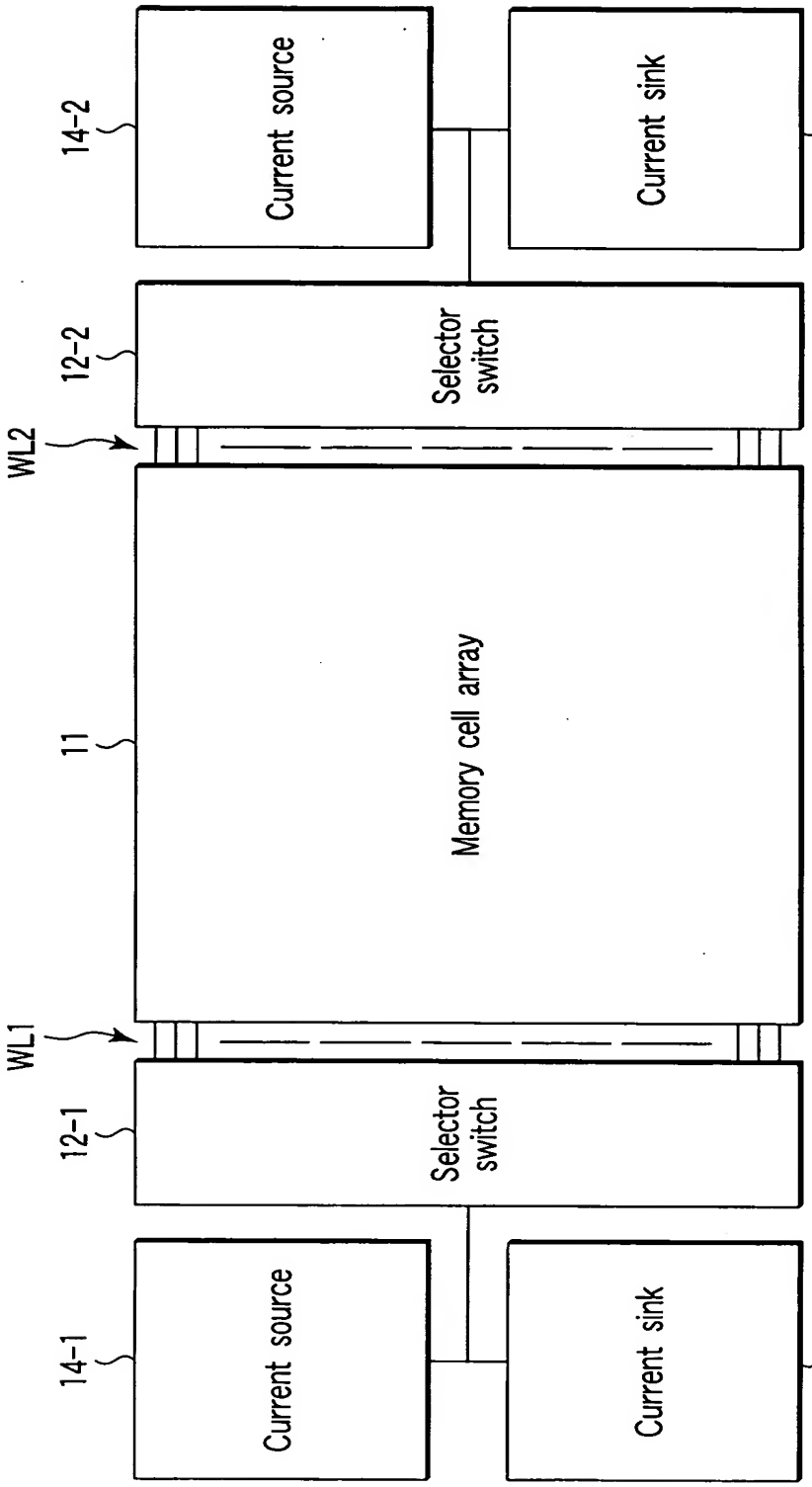
Current source
Current sink
14-2
13-2
Selector switch
12-2
WL2
Memory cell array
11
WL1
Selector switch
12-1
Current source
Current sink
14-1
13-1

FIG. 14

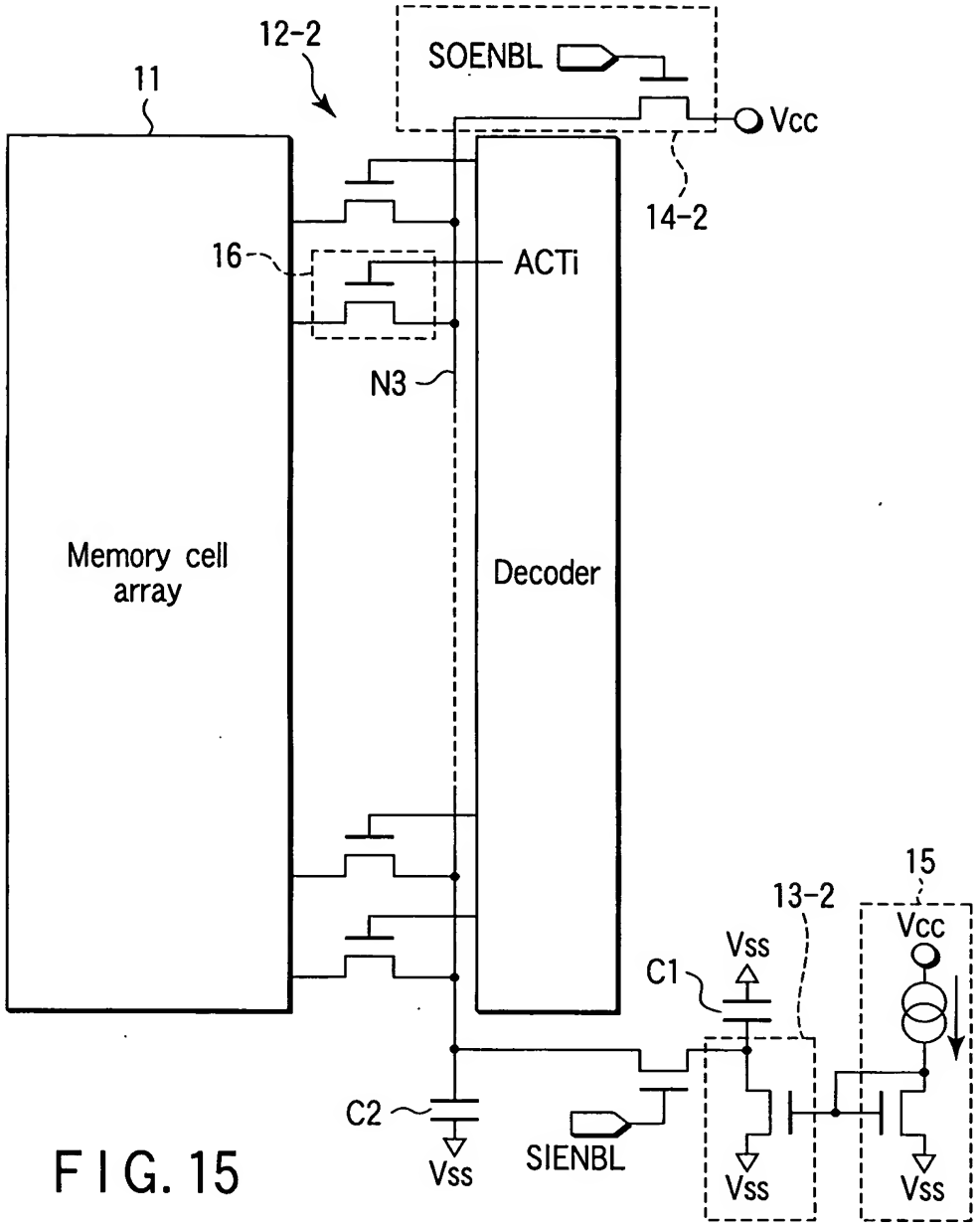
12-2
SOENBL
11
Vcc
14-2
16
ACTi
N3
Memory cell array
Decoder
15
13-2
Vss
C1
Vcc
C2
Vss
SIENBL
Vss
Vss

FIG. 15

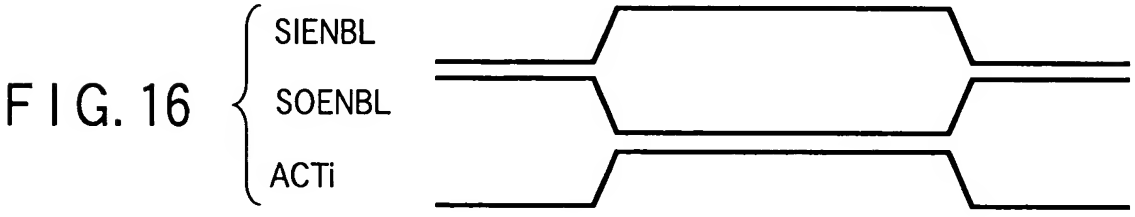
SIENBL
SOENBL
ACTi

FIG. 16

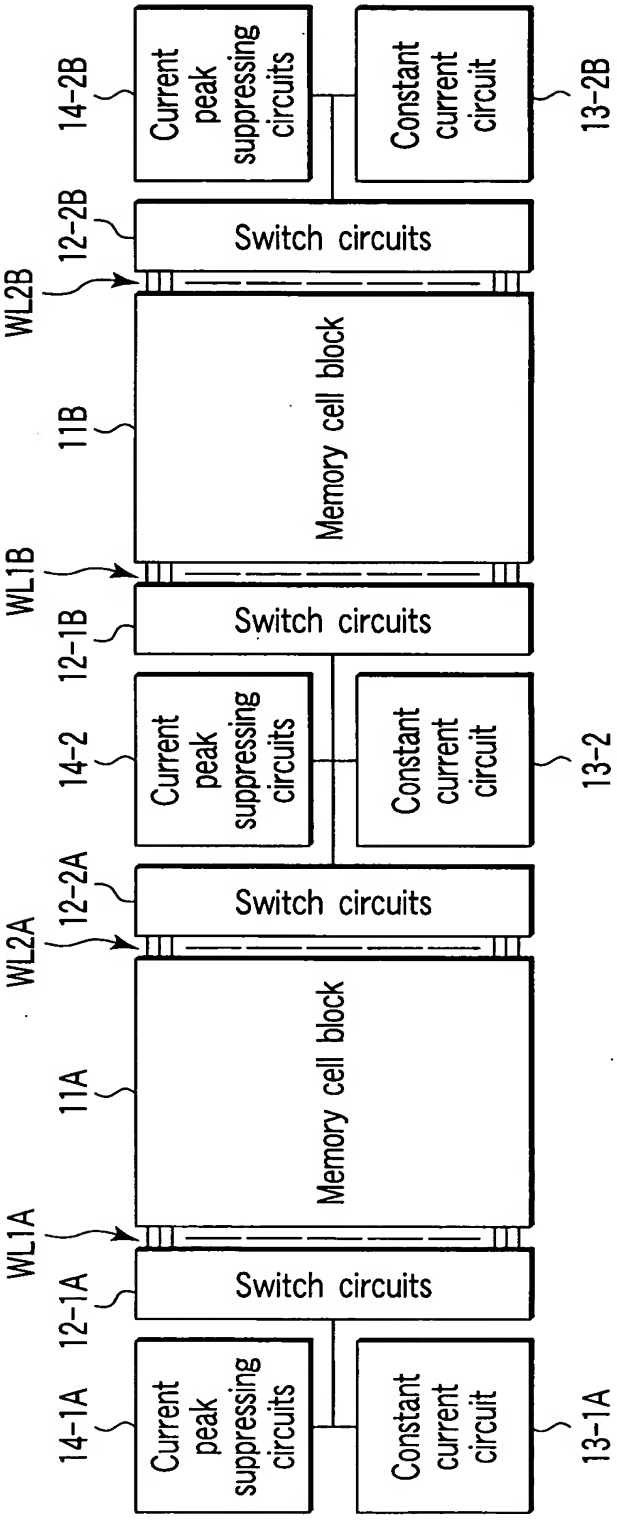
14-2B
Current peak suppressing circuits
Constant current circuit
13-2B
12-2B
Switch circuits
WL2B
11B
Memory cell block
WL1B
12-1B
Switch circuits
14-2
Current peak suppressing circuits
Constant current circuit
13-2
12-2A
Switch circuits
WL2A
11A
Memory cell block
WL1A
12-1A
Switch circuits
14-1A
Current peak suppressing circuits
Constant current circuit
13-1A

FIG. 17

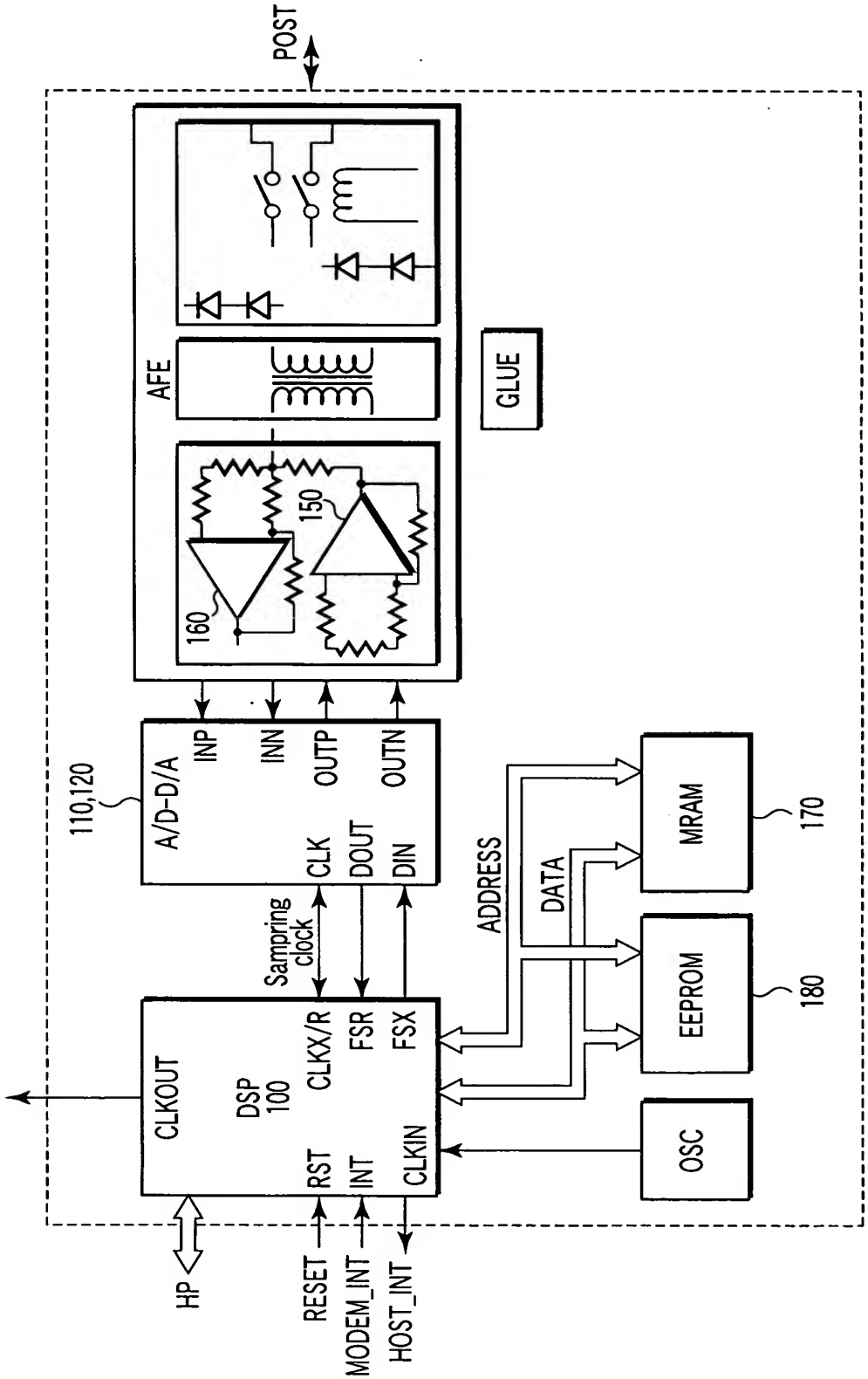
POST
AFE
GLUE
150
160
110,120
A/D-D/A
INP
INN
OUTP
OUTN
CLK
DOUT
DIN
Sampring clock
ADDRESS
DATA
MRAM
170
EEPROM
180
OSC
CLKOUT
DSP 100
CLKX/R
FSR
FSX
RST
INT
CLKIN
HP
RESET
MODEM_INT
HOST_INT

FIG. 18

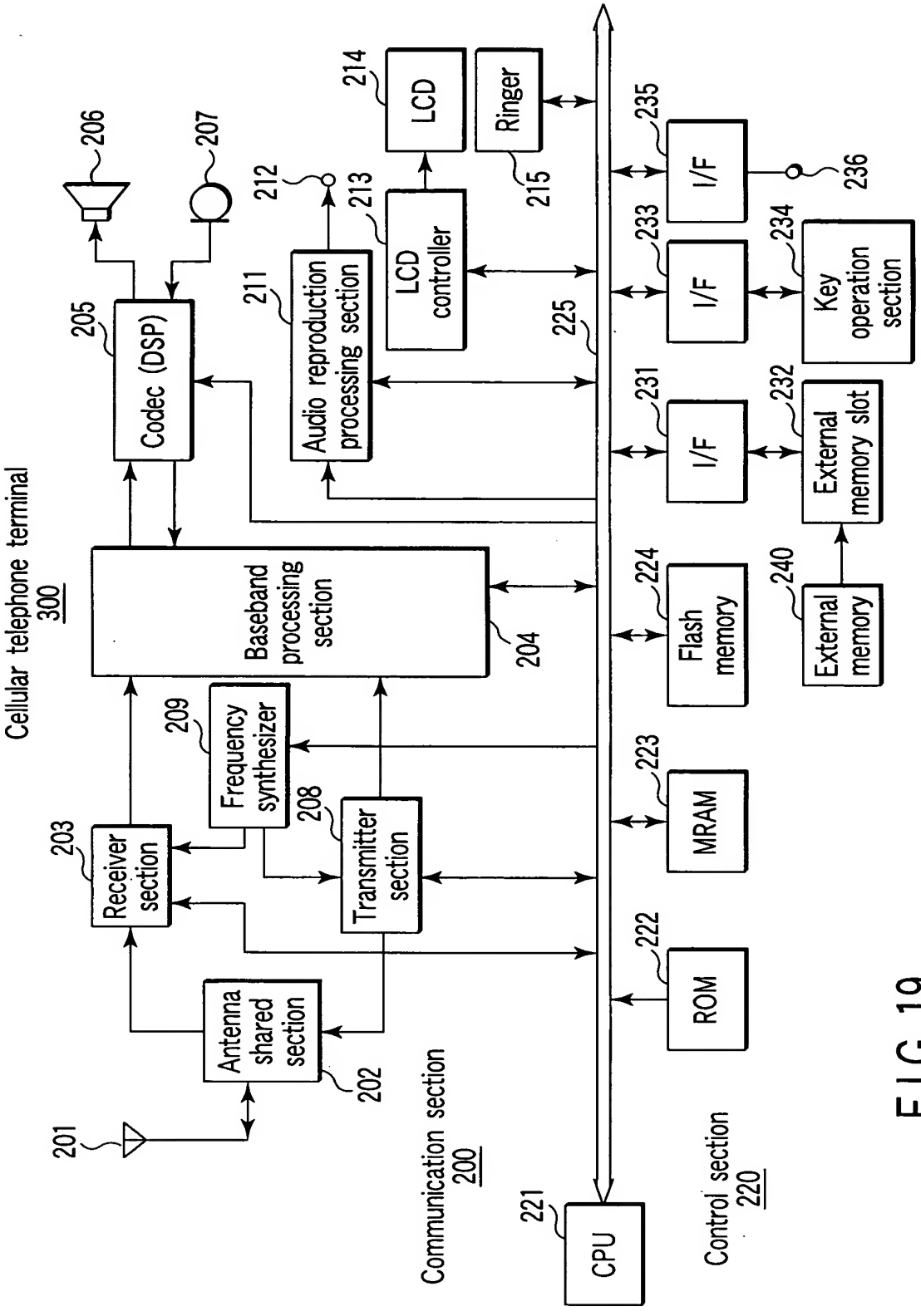
Cellular telephone terminal
300
Communication section
200
Control section
220
Antenna shared section
202
Receiver section
203
Transmitter section
208
Frequency synthesizer
209
Baseband processing section
204
Codec (DSP)
205
Audio reproduction processing section
211
LCD controller
213
LCD
214
Ringer
215
CPU
221
ROM
222
MRAM
223
Flash memory
224
I/F
225
I/F
231
I/F
233
I/F
235
External memory slot
232
Key operation section
234
External memory
240
201
206
207
212
236

FIG. 19

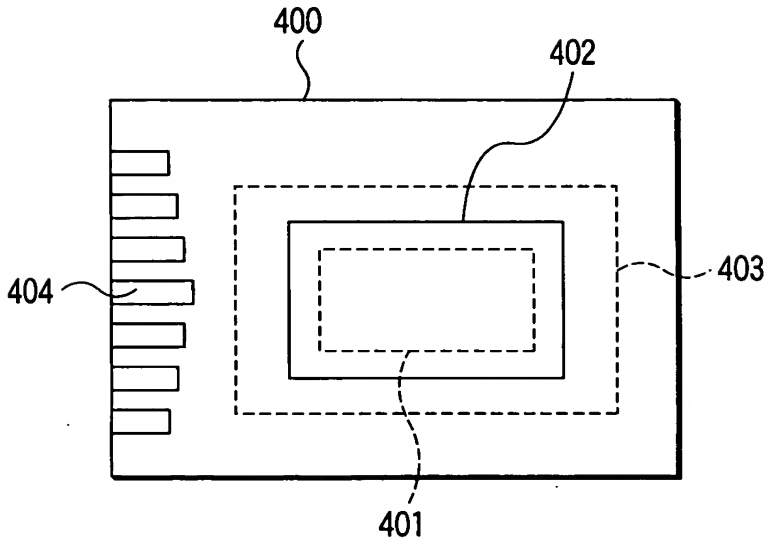
400
402
403
404
401

FIG. 20

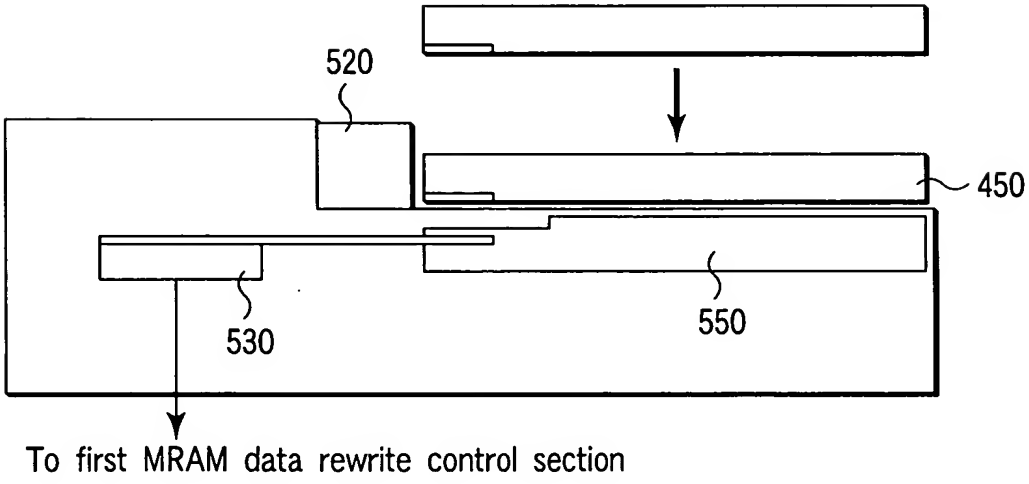
520
450
530
550
To first MRAM data rewrite control section

FIG. 23

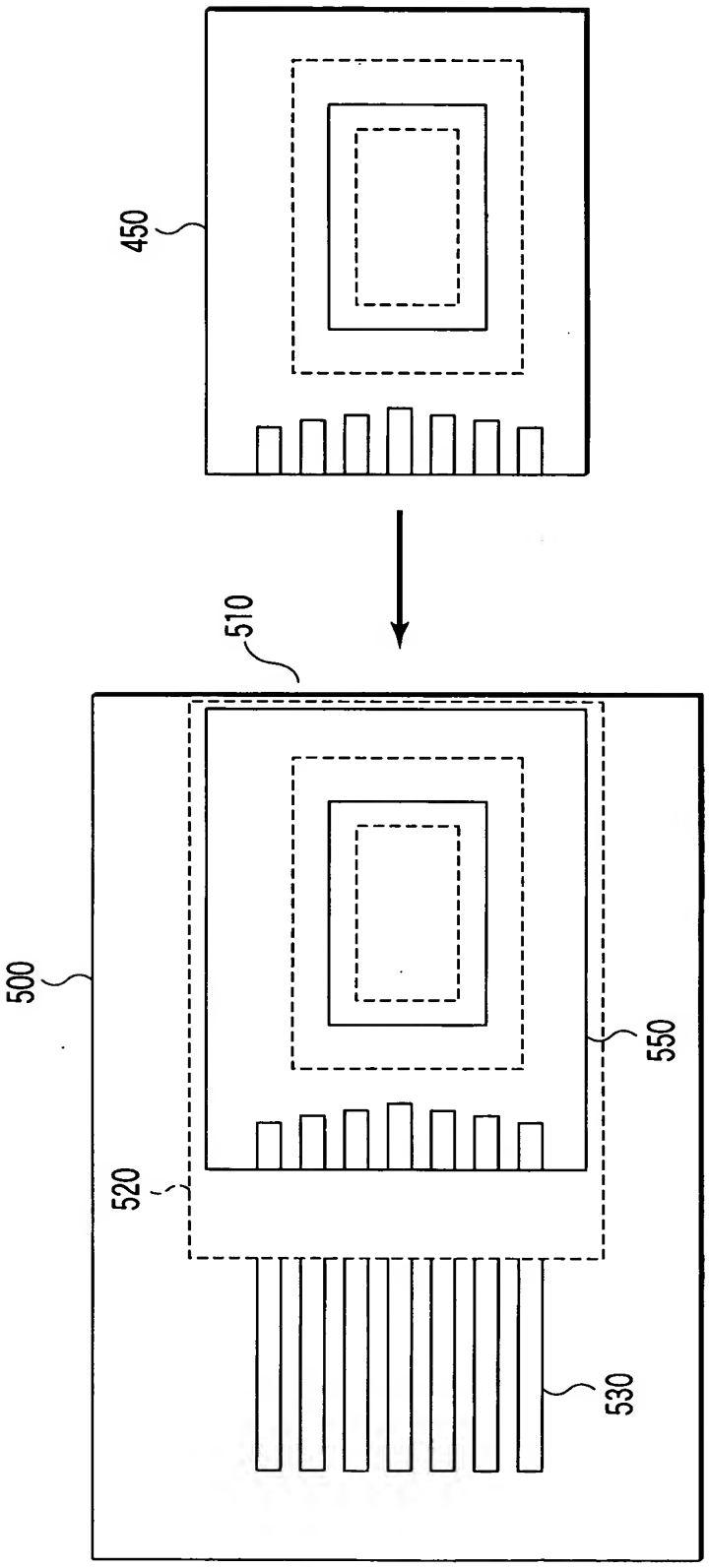

FIG. 21

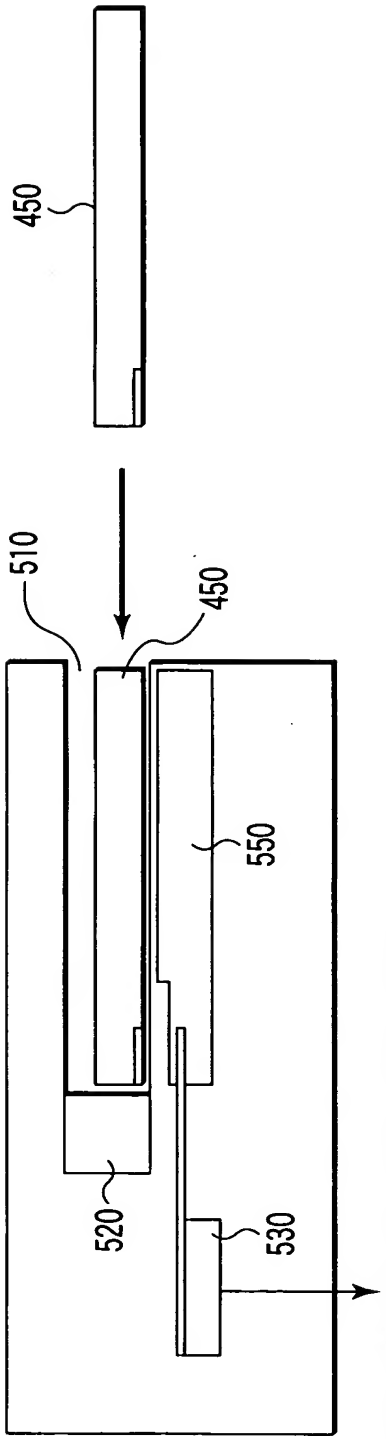
450
510
450
550
520
530
To first MRAM data rewrite control section

FIG. 22

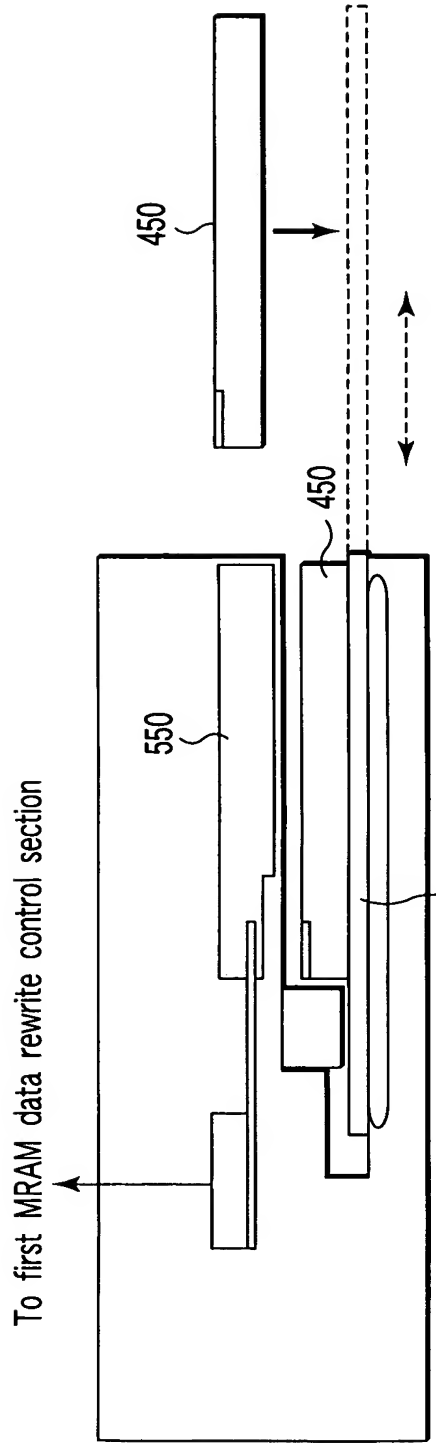
450
450
550
560
To first MRAM data rewrite control section

FIG. 24